What is claimed is:

1. A memory cell structure of a metal programmable ROM, comprising:

a word line;

a bit line;

first and second virtual grounding lines;

a cell transistor having a first side connected to the bit line, wherein the cell transistor provides a first bit cell selected by signals of the word line and the first virtual grounding line and a second bit cell selected by signals of the word line and the second virtual grounding line.

2. The memory cell structure of Claim 1, further comprising a grounding line.

3. The memory cell structure of Claim 2, wherein a second side of the cell transistor is selectively floated or connected to one of the first virtual grounding line, the second virtual grounding line and/or the grounding line, and the gate of the cell transistor is connected to the word line.

4. A memory cell structure of a metal programmable ROM, comprising:

first and second word lines;

a bit line;

a grounding line;

first and second virtual grounding lines;

a first cell transistor having a drain connected to the bit line and a gate connected to the first word line; and

a second cell transistor having a drain connected to the bit line and a gate connected to the second word line.

5. The memory cell structure of Claim 4, wherein a source of the first cell transistor is floated or connected to one of the first virtual grounding line, the second virtual grounding line and/or the grounding line.

6. The memory cell structure of Claim 4, wherein a source of the second cell transistor is floated or connected to one of the first virtual grounding line, the second virtual grounding line and/or the grounding line.

7. The memory cell structure of Claim 4, wherein the first cell transistor is shared by both a first bit cell selected by the first word line and the first virtual grounding line and a second bit cell selected by the first word line and the second virtual grounding line.

8. The memory cell structure of Claim 4, wherein the second cell transistor is shared both by a third bit cell selected by the second word line and the first virtual grounding line and a fourth bit cell selected by the second word line and the second virtual grounding line.

9. A memory cell structure of a metal programmable ROM, comprising:

first and second word lines;

first and second bit lines;

a grounding line;

first, second and third virtual grounding lines;

a first cell transistor having a drain connected to the first bit line and a gate connected to the first word line;

a second cell transistor having a drain connected to the first bit line and a gate connected to the second word line;

a third cell transistor having a drain connected to the second bit line and a gate connected to the first word line; and

a fourth cell transistor having a drain connected to the second bit line and a gate connected to the second word line.

10. The memory cell structure of Claim 9, wherein a source of the first cell transistor is floated or connected to one of the first virtual grounding line, the second virtual grounding line and/or the grounding line and a source of the second cell transistor is floated or connected to one of the first virtual grounding line, the second virtual grounding line and/or the grounding line.

11. The memory cell structure of Claim 9, wherein a source of the third cell transistor is floated or connected to one of the second virtual grounding line, the third virtual grounding line and/or the grounding line and a source of the fourth cell transistor is floated or connected to one of the second virtual grounding line, the third virtual grounding line and/or the grounding line.

12. The memory cell structure of Claim 9, wherein the first cell transistor is shared both by a bit cell selected by the first word line and the first virtual grounding line and a bit cell selected by the first word line and the second virtual grounding line.

13. The memory cell structure of Claim 9, wherein the second cell transistor is shared both by a bit cell selected by the second word line and the first virtual grounding line and a bit cell selected by the second word line and the second virtual grounding line.

14. The memory cell structure of Claim 9, wherein the third cell transistor is shared both by a bit cell selected by the first word line and the second virtual grounding line and a bit cell selected by the first word line and the third virtual grounding line.

15. The memory cell structure of Claim 9, wherein the fourth cell transistor is shared by both a bit cell selected by the second word line and the second virtual grounding line and a bit cell selected by the second word line and the third virtual grounding line.

16. A memory cell structure for two bit cells of a programmable ROM, comprising:

a word line;

a bit line;

a grounding line;

first and second virtual grounding lines; and

a transistor having a controlling terminal connected to the word line, a first controlled terminal connected to the bit line and a second controlled terminal selectively floated or connected to one of the grounding line, the first virtual grounding line, the second virtual grounding line or the bit line based on a value of data programmed into the two bit cells.

17. The memory cell structure of Claim 16, wherein the second controlled terminal of the transistor is floated or connected to the bit line to program both bit values to a first logic value.

18. The memory cell structure of Claim 17, wherein the second controlled terminal is connected to the grounding line to program both bit values to a second logic value opposite the first logic value.

19. The memory cell structure of Claim 18, wherein the second controlled terminal is connected to the first virtual grounding line to program a value of the first bit cell to the second logic value and the value of the second bit cell to the first logic value or connected to the second virtual grounding line to program a value of the first bit cell to the first logic value and the value of the second bit cell to the second logic value.

20. The memory cell structure of Claim 16, wherein the second controlled terminal is selectively floated or connected by a metal fabrication process.

21. The memory cell structure of Claim 16, wherein the second controlled terminal is selectively floated or connected by the selective formation of vias.